Localized SOI for monolithic integration of silicon photonics, IC and MEMS

Nano Innovation 2016 Rome, 20-23 September
Conference & Exhibition

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Agenda / Outline / Overview

- Introduction
- Silicon Photonic (SP), SP platform, SP roadmap
- SP issues
- Technology solutions for real monolithic SP and IC integration
- Porous Silicon (PS) and OPS
- Porous Silicon: Localized Processing by DLD/DLM
- Our approach to SP by OPS
- Results and ongoing work
- Summary & Conclusions

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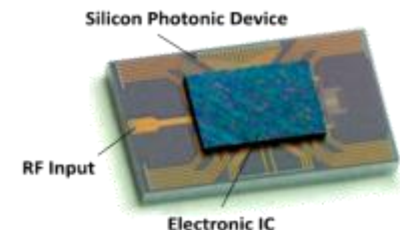
Introduction

- Integrated Optics (IO)
  - with the meaning of optical devices and circuits realized in a patterned planar waveguide format, was first described by Stewart Miller in a historic special issue of the Bell System Technical Journal (BSTJ), as long ago as 1969
  - Miller envisaged an analogous development to Integrated Electronics with a continuously growing density of integration (Moore's law)

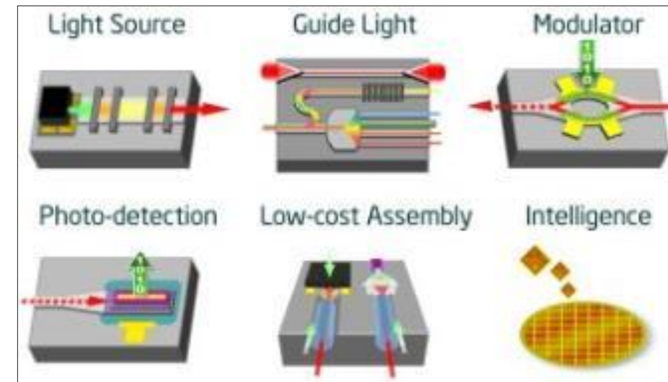
- Integration density in the optical domain was much slower than in electronics
  - IC has one dominant material: Silicon
  - IO has wide range of materials:
  - e.g. $LiNbO_3$ optical modulator are among the key components that enable the today worldwide optical internet

- Silicon but currently only in the form of silicon-on-insulator (SOI)
  - has emerged during the last few years as a strong contender for various applications of Integrated Optics



Silicon Photonic (SP)

SP Kick-off: The first multi-Gb/s capable silicon photonics modulator was reported in 2004 by Intel



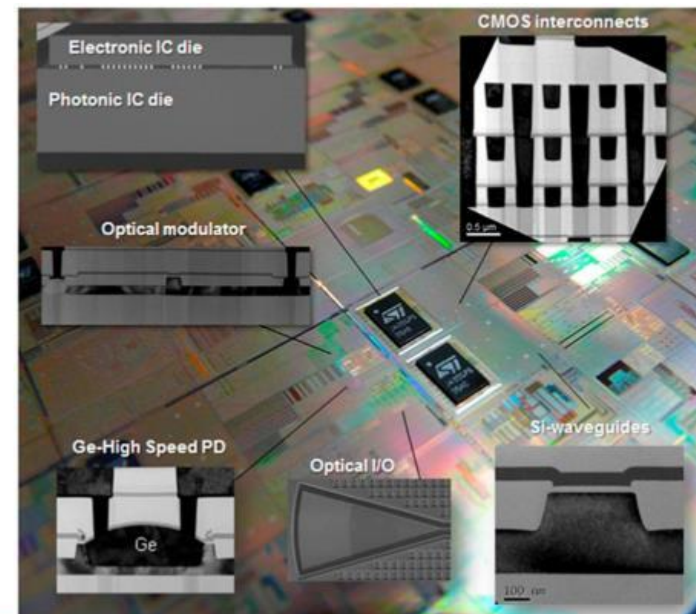
Intel-labs-SP-Six-Building-Blocks

Since then, SP has seen an explosion of interest

- Low-loss waveguides (Caltech, 2005)
- Grating Couplers (Gent and IMEC, 2010)
- Ge Detectors in Si by SANDIA, MIT and IQE Silicon Compounds (2011)
- Optical modulators by Intel 2004

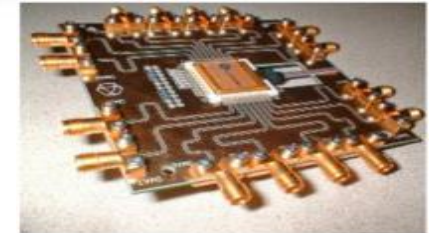
All separately demonstrated

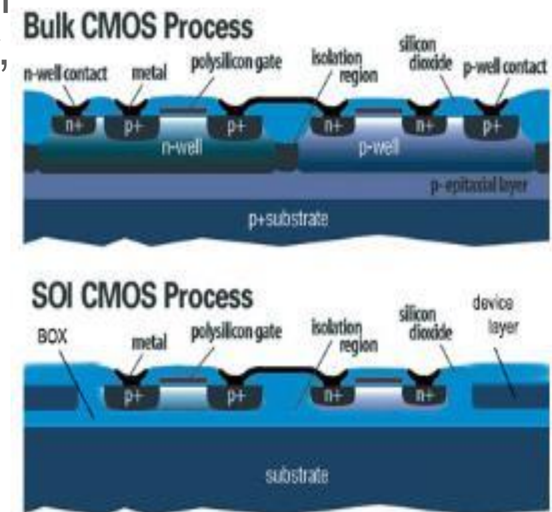
The challenge is to Develop a platform that supports all of these key components simultaneously with attractive performance, and achieves drive voltages compatible with CMOS processes



SP platform

- **Luxtera** in 2011 demonstated 25 Gb/s capability and recently reported a 4x28G link.
  - the technical details remain unpublished
  - key device geometries and performance kept in secret
- **ePIXfab** has been providing fabrication services to the photonics community, and has published results on modulators and detectors for 40 Gb/s speeds separately, though no results achieved simultaneously as a part of an integrated platform
- A wafer-scale SP platform demonstrated achieving 15 GHz bandwidths capable of 25 Gb/s data rates using an SOI wafer with a very high resistivity handle layer (i.e. **750 Ω·cm**)
  - Traveling wave modulator made with a special structure to mainly allow current pass trough the metal and not in silicon to ensure that RF losses remain low
  - Driving circuits where not integrated


Luxtera's 10Gbit Device on Test Board



- **Intel** and **IBM** have reported individual high-performance devices. J. Trewhella **IBM** (ECTC 2014) announced monolithic SP and CMOS IC @ 90nm – 65 nm (Max 10Gbps)!!!!
- P. De Dobbelaere from **Luxtera** (ECTC 2014) showed that they give up on monolithic integration of SP and IC

SP Roadmap

- Silicon photonics (SP) technology envisions a clear road map fitting the needs and the challenges of the future ICT (Information Communication Technology) systems and services.

- Key applications driving the SP:
  - high performance computing,
  - broadband communication,
  - mass storage
  - consumer multimedia

	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Others	$0	$0	$0	$0	$0	$0	$0	$1	$2	$2	$4	$5
Telecom / Datacom	$23	$26	$32	$32	$31	$34	$37	$36	$45	$52	$63	$70
Data Centres	$0	$0	$0	$0	$0	$54	$106	$208	$252	$292	$329	$410
HPC	$0	$3	$8	$14	$21	$34	$45	$85	$146	$189	$216	$235
TOTAL	$23	$29	$39	$46	$52	$122	$188	$330	$444	$535	$612	$720

Still many key technological breakthroughs are needed to enable the **intra-chip interconnections**

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SP Roadmap

28nm technology node IC is in *bulk CMOS (Intel)* or *FDSOI (Samsung and STM)*

450 mm Si wafer in production from 2018

Silicon Photonics Roadmap

Silicon photonic generation		I	II	III	IV
Year		2012	2015	2018	2021
Application		Active Cables	Active cables Opto Modules	Opto Modules 2D/3D Opto Asics	Opto Asics Opto Chip
Technology Breaktrough		Reference	CMOS 65nm Electronics	CMOS 28nm µRing Resonator WDM (4λ)	CMOS 15nm µLaser DWDM (16λ) 3D Packaging & Cooling
Data Rate per link		10 Gbps	30 Gbps	200 Gbps	800 Gbps
Aggregate Bandwidth		40 Gbps	120 Gbps	800 Gbps	3200 Gbps
Parallel Link (4λ)	Estimated Energy/bit	< 20 pJ/bit	< 12 pJ/bit	< 3 pJ/bit	< 1 pJ/bit
	Estimated Size/module	10.000 mm3	10.000 mm3	5.000 mm3	150 mm3
	Estimated cost/module	4 $/Gbps	1.33 $/Gbps	0.32 $/Gbps	0.04 $/Gbps

M.Zuffada: “The industrialization of the Silicon Photonics: technology road map and applications” Solid-State Device Research Conference (ESSDERC), 2012

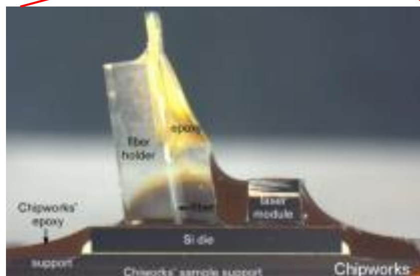
Proceedings of the European, 17-21 Sept. 2012, pp. 7-13

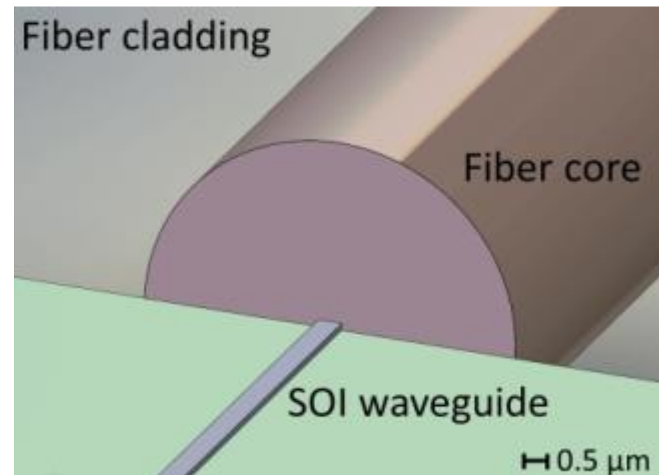
SP issues: SMF coupling

http://www.helios-project.eu/Download/Public-deliverables
document: D010 State of the art, last update

Fiber coupling structures	3D adiabatic tapers	Anti-resonant reflecting optical waveguides	Adiabatic inverse tapers	1D and 2D fiber grating couplers
Insertion loss with SMF	< 1dB Sensitive to reflections	< 1dB HNA fiber required (typ. ∅mode3μm)	< 0.5dB HNA fiber required (typ. ∅mode3μm)	1D : about 1.6 dB 2D : about 6dB
Alignment tolerance	++	+	+	++
Spectral bandwidth	broadband	< 2nm	several 100nm	several 10nm
Polarization sensitivity	no	yes	yes but depending on the tip width	1D : yes 2D : no
Coupling configuration	planar	planar	planar	non planar
Fabrication issue	edge of the chip optical quality and antireflective coating	edge of the chip optical quality	edge of the chip optical quality	no specific issue
Testing issue	non compatible with wafer-scale testing	non compatible with wafer-scale testing	non compatible with wafer-scale testing	compatible with wafer-scale testing
Industrial application	3μm to 10μm spot size converter			submicron to 10μm spot size converter

The Luxtera CMOS Integrated Photonic Chip in a Molex Cable





NEC Corporation presented a new **vertical-coupling optical interface** [*]

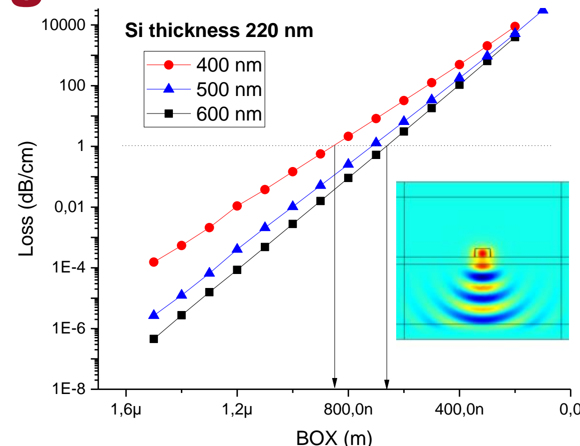
- grating coupler - SMF and SiWG
- coupling efficiency of ~50% at 850nm
- Tolerance misalignment (+1dB losses): 1.5μm, ±2μm in the x-, z- directions
- they claim to reach the same value for 1550nm

[*] Hirohito Yamada et al., “ Vertical-coupling optical interface for on-chip optical interconnection” OPTICS EXPRESS (2011) Vol. 19, No. 2 pp. 698-703

SP issues: Monolithic Integration

Main issues for real monolithic integration of SP and IC

- SOI wafer are 8nm TopSi and 25 nm BOX have nothing to deal with SOI for silicon photonics. SOI wafers for photonics need thick BOX (i.e. > 1 micron) this means thermal issues for fast IC!



Low box = high leakage

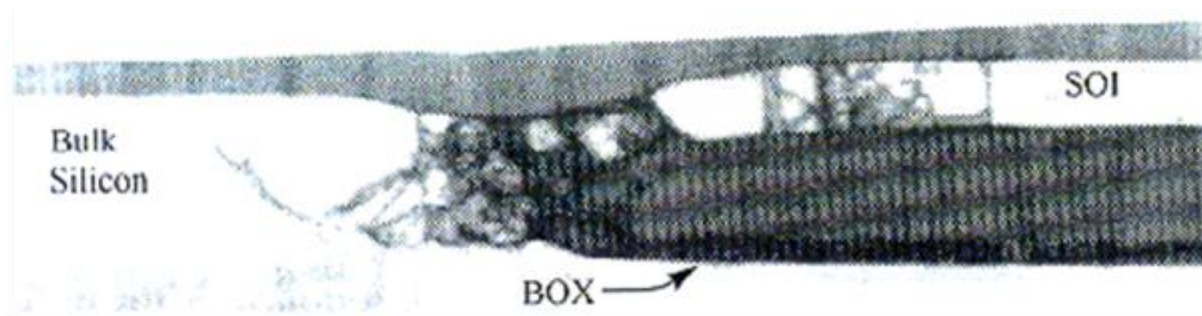
- The IC chips for data rates above 100Gbps are in SiGe or SiGe:C or CMOS 60nm (→45nm) built in bulk silicon not in SOI

- Silicon photonics devices are quite sensitive to uniformity of SOI wafers TopSi within wafer and within wafer to wafer (i.e. IMEC developed process to increase uniformity of TopSi of SOI wafer). Furthermore, handle SOI must be with very high resistivity

Localized SOI is the obvious solution

Technology solutions for real monolithic SP and IC integration

- Can we modulate BOX and TopSi thickness by Oxygen implantation on the same wafer?
  - implanter can give better than 1,5% (3σ) uniformity of dose distribution within wafer-to-wafer and different wafer runs
- Can we have localized SOI only where we need SP?



Ref. : "SOI Circuits Design Concept", H. Bernstein, N.J. Rohrer ***IBM Microelectronics****, 2000*

THE ANSWER IS

NO!

Technology solutions for SP

Is there a solution for Localized SOI Structures ?

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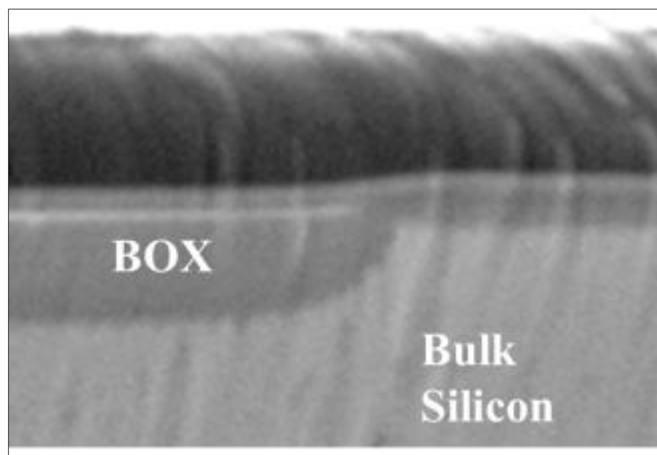
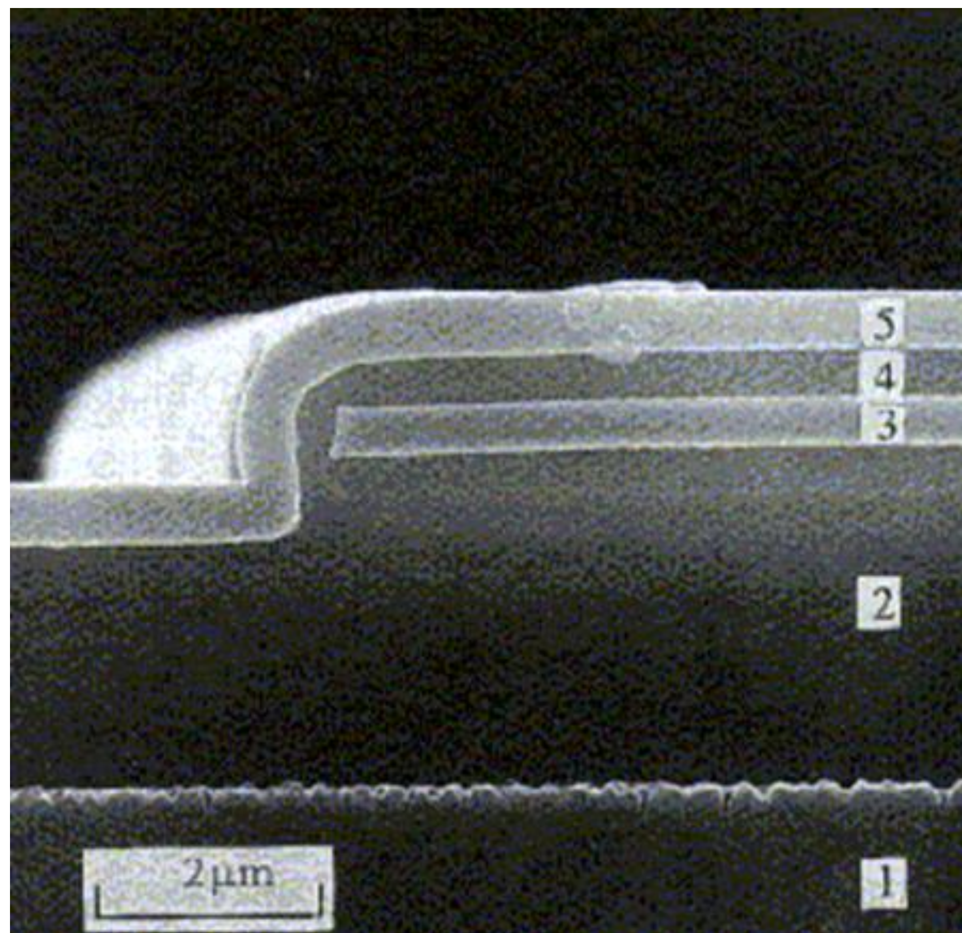
Technology solutions for SP

YES: Use of Porous Silicon and Oxidation

1. Bulk Silicon
2. Densified Oxidized Porous Silicon (1200nm)
3. Silicon (n type 400nm)
4. Oxide (320nm)
5. PolySilicon (480nm)



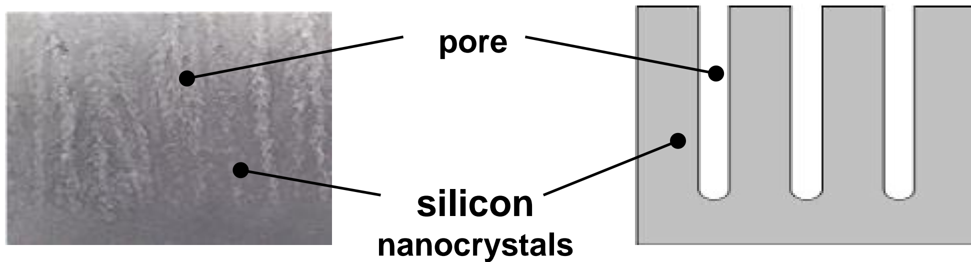


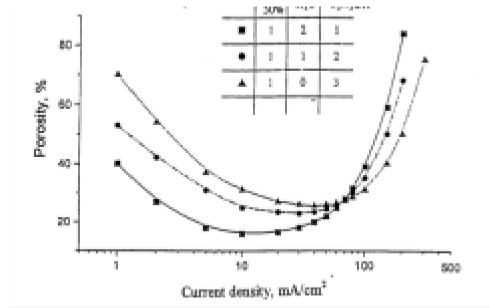
Arthur Uhlir and Ingeborg Uhlir
Mother and Father of Porous Silicon

The first porous silicon was discovered in 1956 in room 2B102 of the Bell Lab at Murray Hill while study an electropolishing of Si in HF acid.

Porous silicon: basics

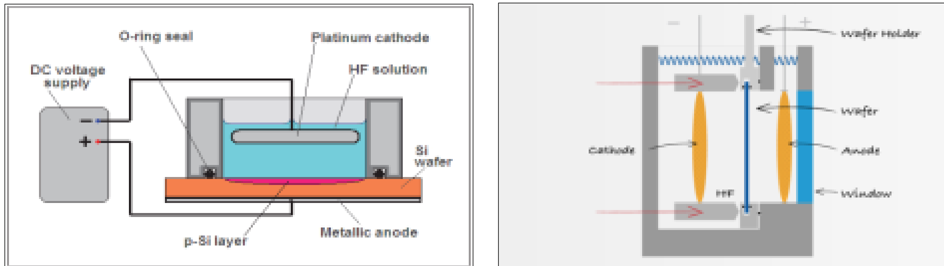
PS can be formed by anodic treatment of monocrystalline Si in HF-based solution

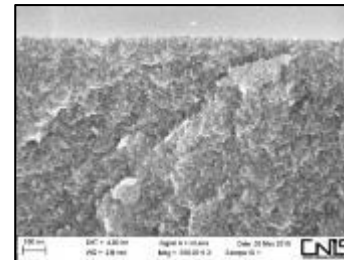


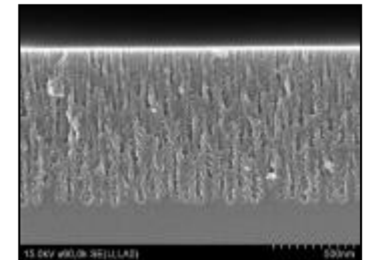


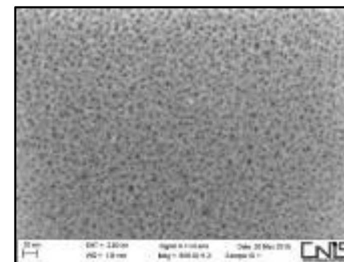
Various morphologies:
from **nanoporous** to **macroporous**
From 0% to 95%

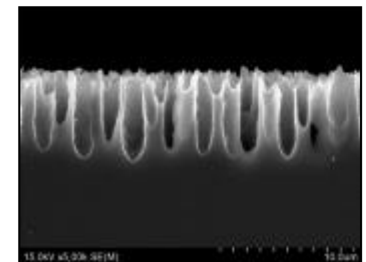
Principle of electrochemical cell used for PS











Localized PS is usually made using HF-resistant mask (Si_3N_4, noble metals)

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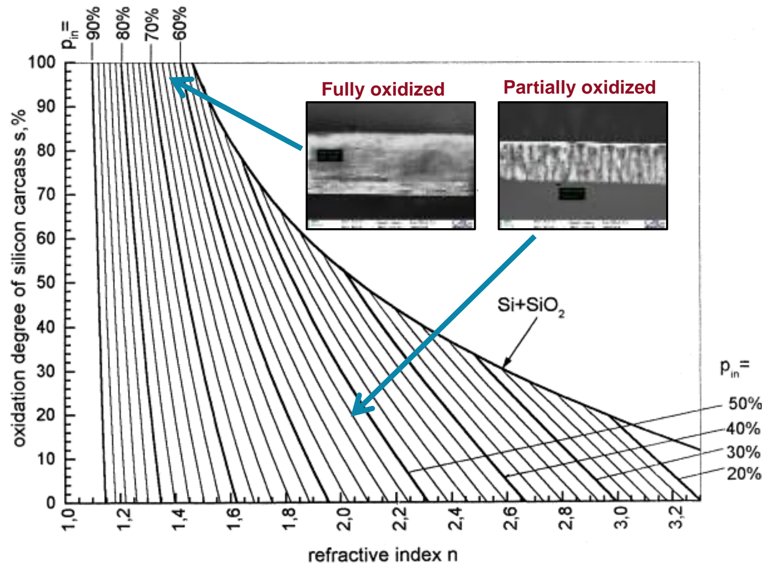
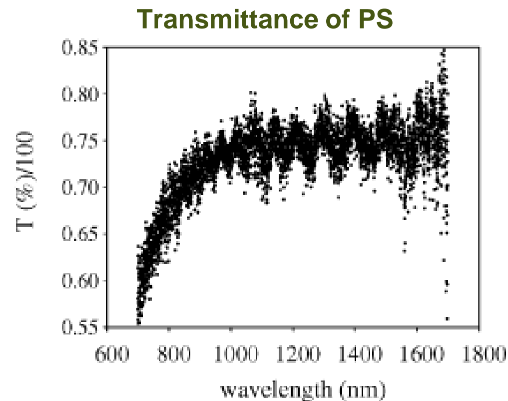
Porous silicon: oxidation

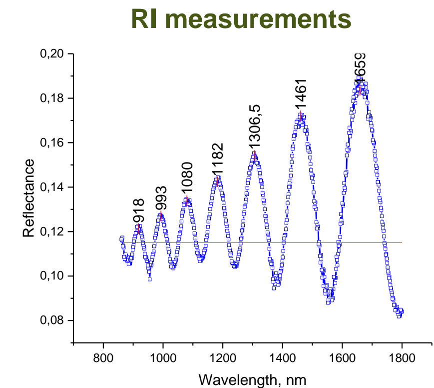


OPS refractive index vs oxidation degree

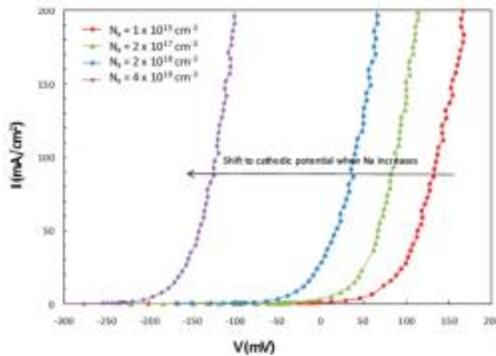
Porosity must be controlled to compensate volume expansion during oxidation

PS is a way to locally transform Si substrate into SP material with optical properties different from those of bulk silicon.
Process is fully compatible with CMOS technology.





Porous silicon: selectivity



Anodic IV characteristics of p-type silicon in HF solution for different doping

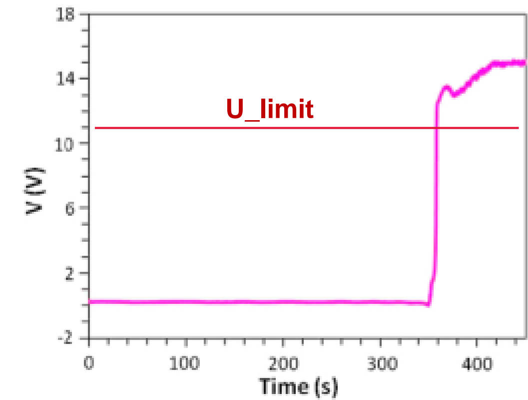
PS needs holes to be formed!

Depending on doping more easy to form PS for:

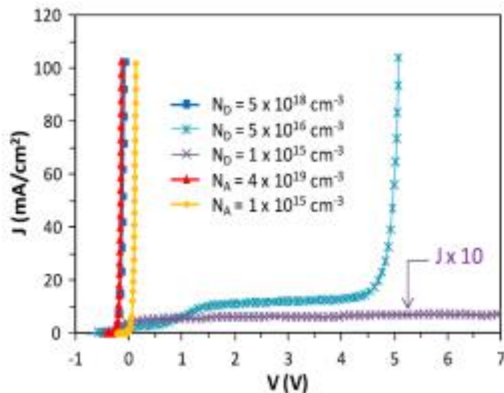
- n^{++} (> $5 \cdot 10^{17}$ atm/cm³)
- p^{++} (> $1 \cdot 10^{19}$ atm/cm³)
- n^{++}<p ($1 \cdot 10^{15}$ atm/cm³)
- p<n ($5 \cdot 10^{16}$ atm/cm³)
- n<n⁻ ($1 \cdot 10^{15}$ atm/cm³)

≅

Increase V



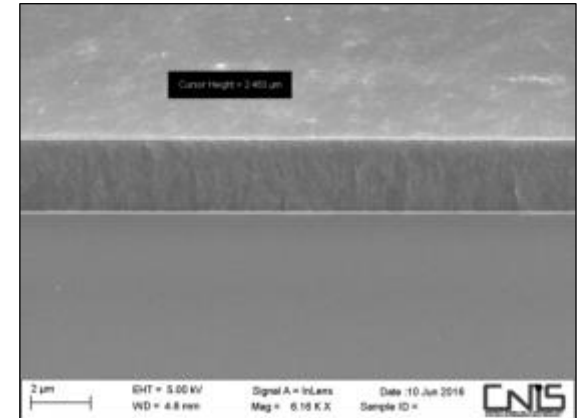
Anodic potential variation during anodization of a sample with N+ layer over N- substrate



Anodic IV characteristics of n- and p-type silicon in HF solution for different doping

By limiting anodization voltage a self-stopping process can be realized

Hydrogen Implant prevents PS formation



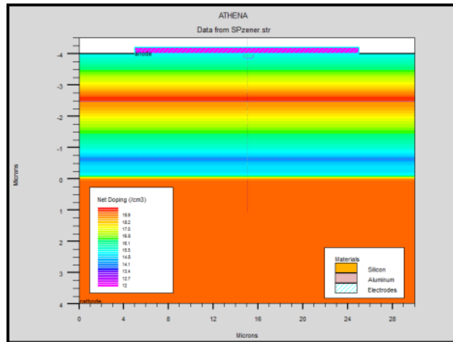
Self-stopping anodization process. The thickness of PS layer equal to N+ layer thickness

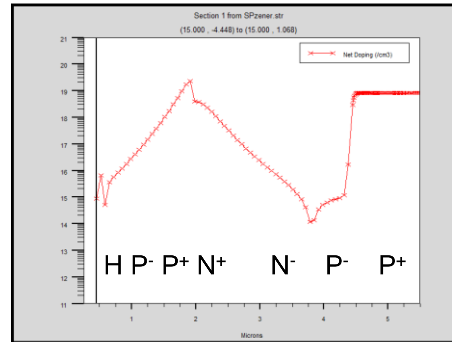
A. Gharbi, B. Remaki, A. Halimaoui, D. Bensahel, and A. Souifi, **"Shallow trench isolation based on selective formation of oxidized porous silicon,"** in *Microelectronic Engineering*, 2011

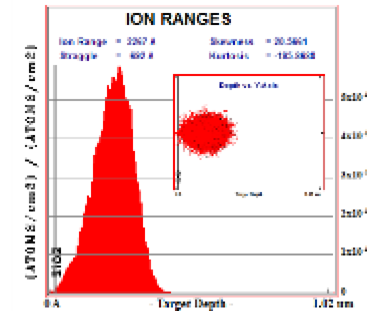
Our approach: buried localized OPS

Key steps

- Smart doping for auto-stop process

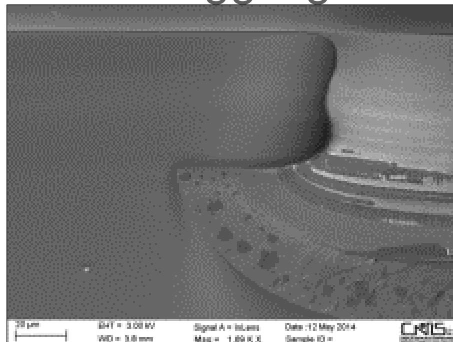


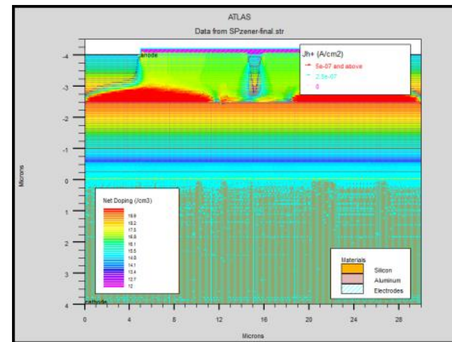


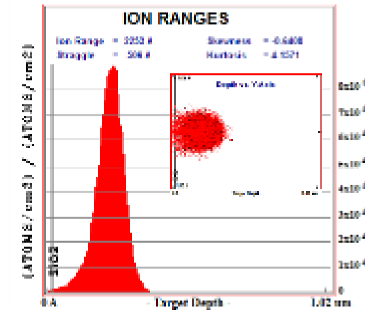


Phosphorous @ 170 keV
220nm/70 nm straggle

- Proton implantation for anozidation selectivity and low straggling



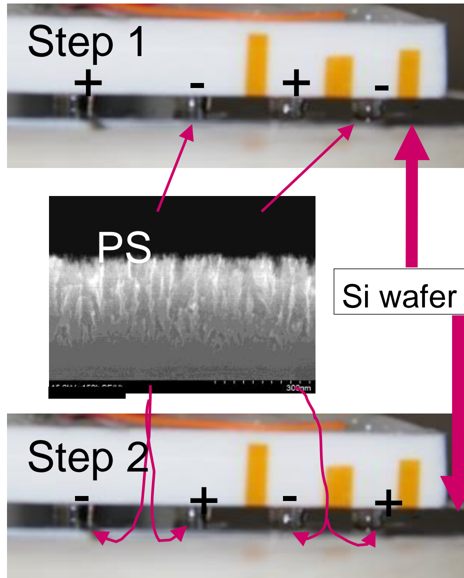


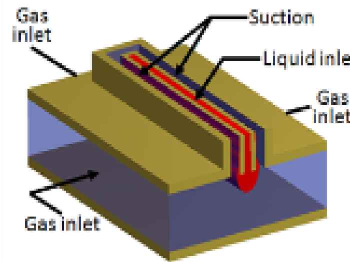


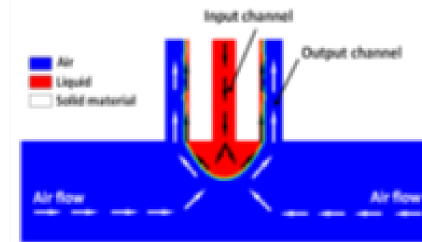
Hydrogen @ 20 keV
220nm/50 nm straggle

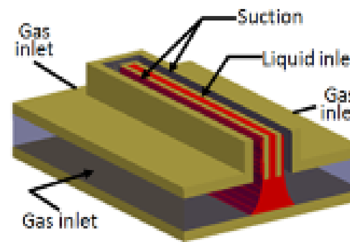
Our aproach: localized Processing by DLD/DLM

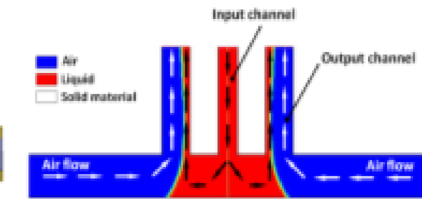
Dynamic Liquid Drop (DLD)/Dynamic Liquid Meniscus (DLM)



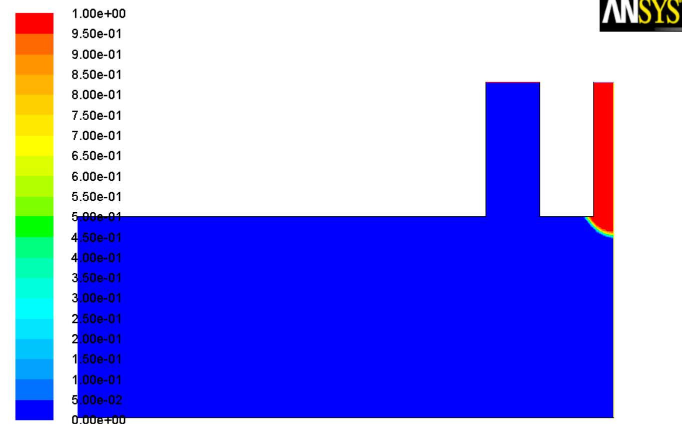




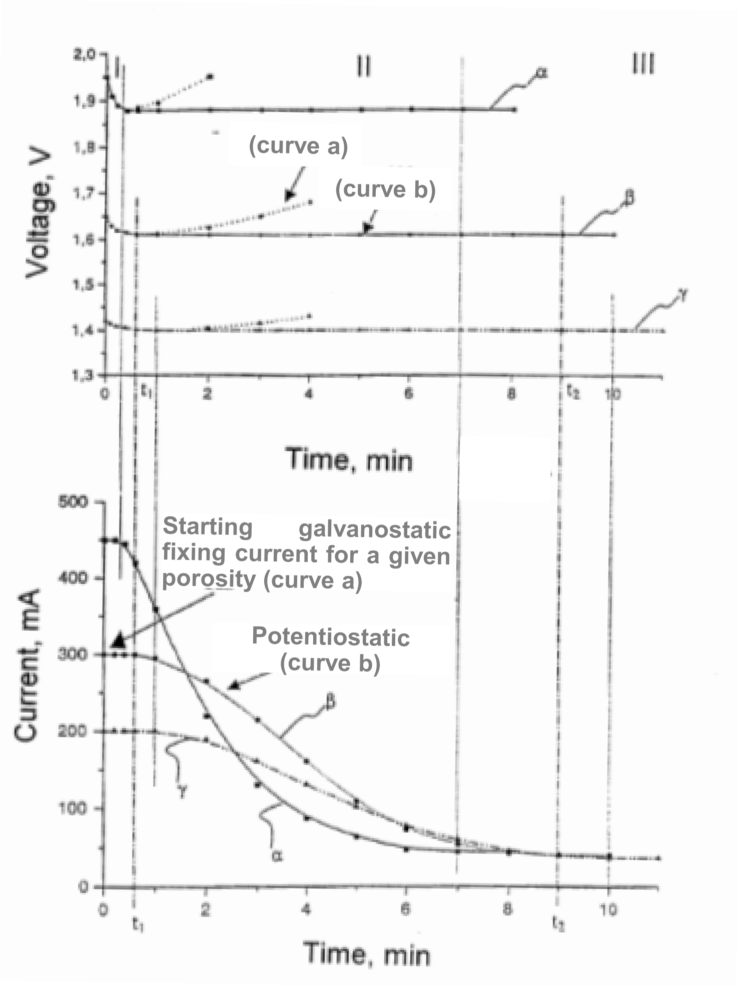


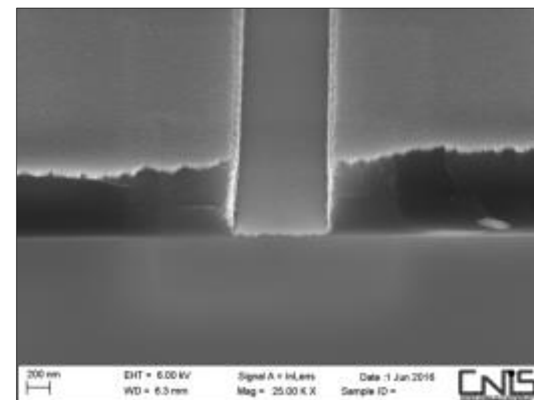


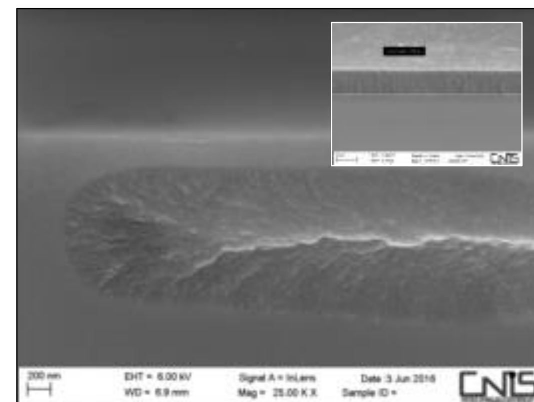
This technique allows to realize without lithography on the same wafer localized PS structures changing: Type of Solution, Current or Voltage, Time influencing PS Morphology, Porosity and Thickness



Results and ongoing work

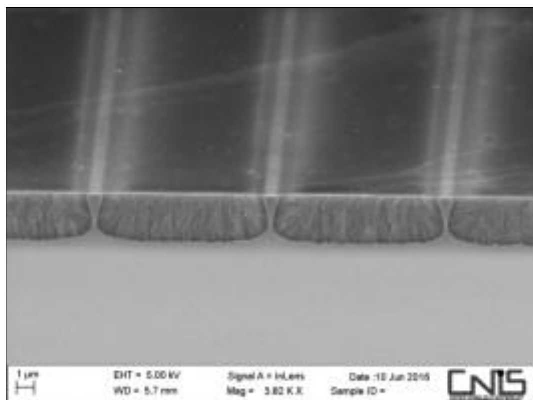


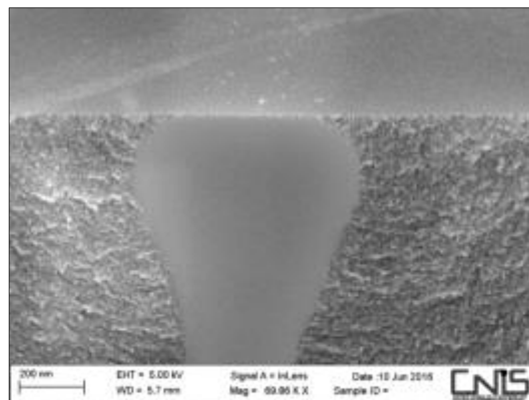


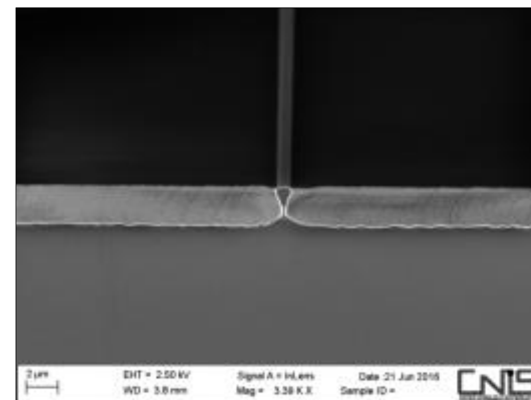


Localized underetching under H-implanted island

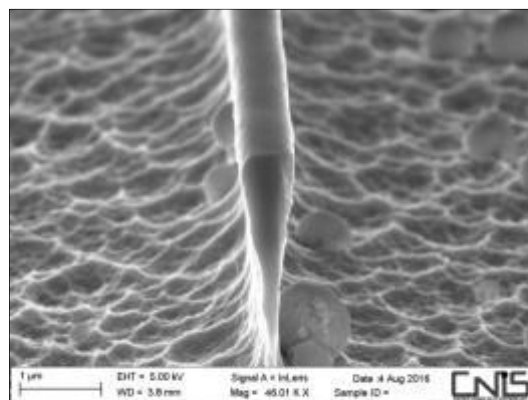
Results and ongoing work

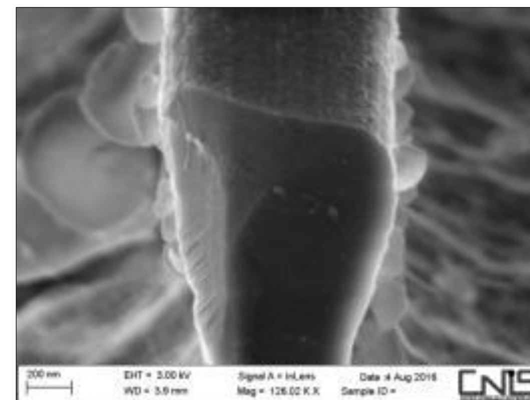






Sidewall roughness studies

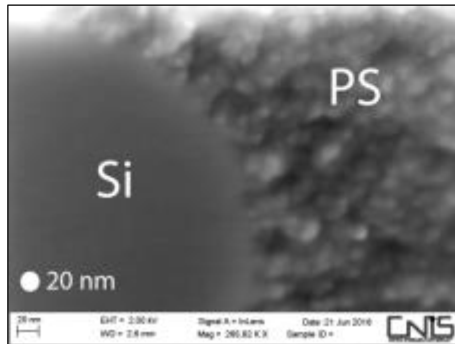


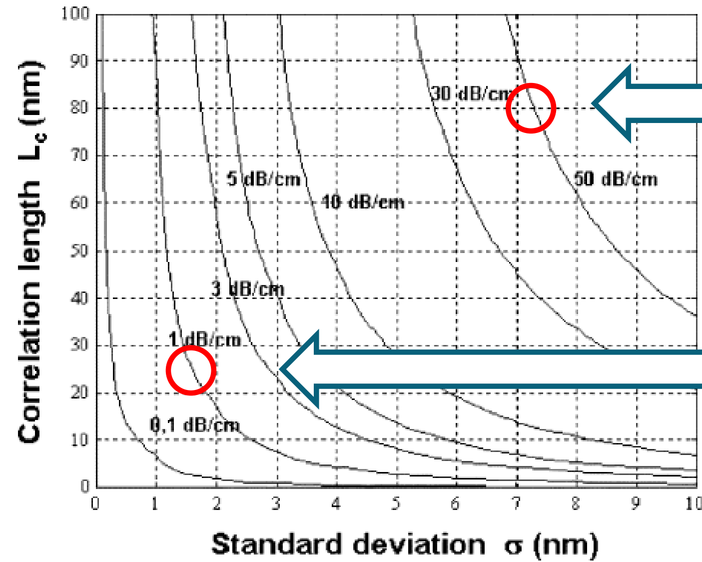


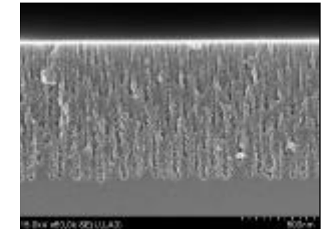
Results and ongoing work: sidewall roughness

Sidewall roughness induced losses are critical for SP!

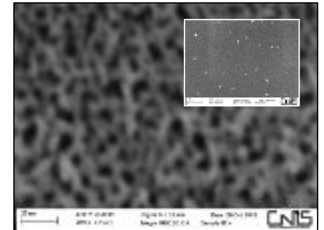
- Low-doped Si favors nanoporous silicon formation. Smaller pores mean lower interface roughness



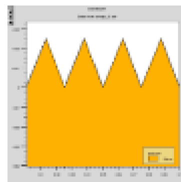




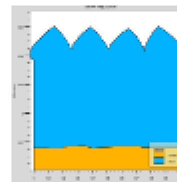
FIPOS: mesoPS, >20 nm



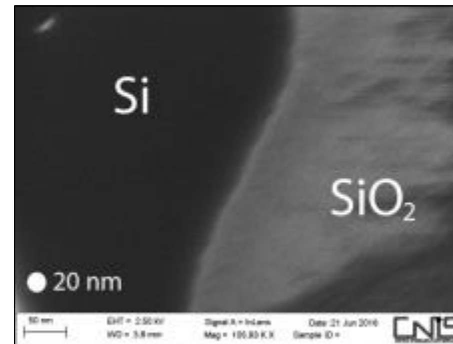
H: nanoPS, <5nm

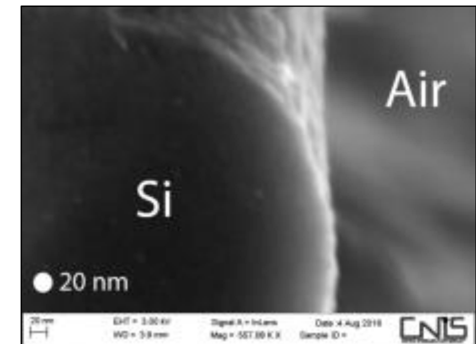


Oxidation process is further decreasing the roughness



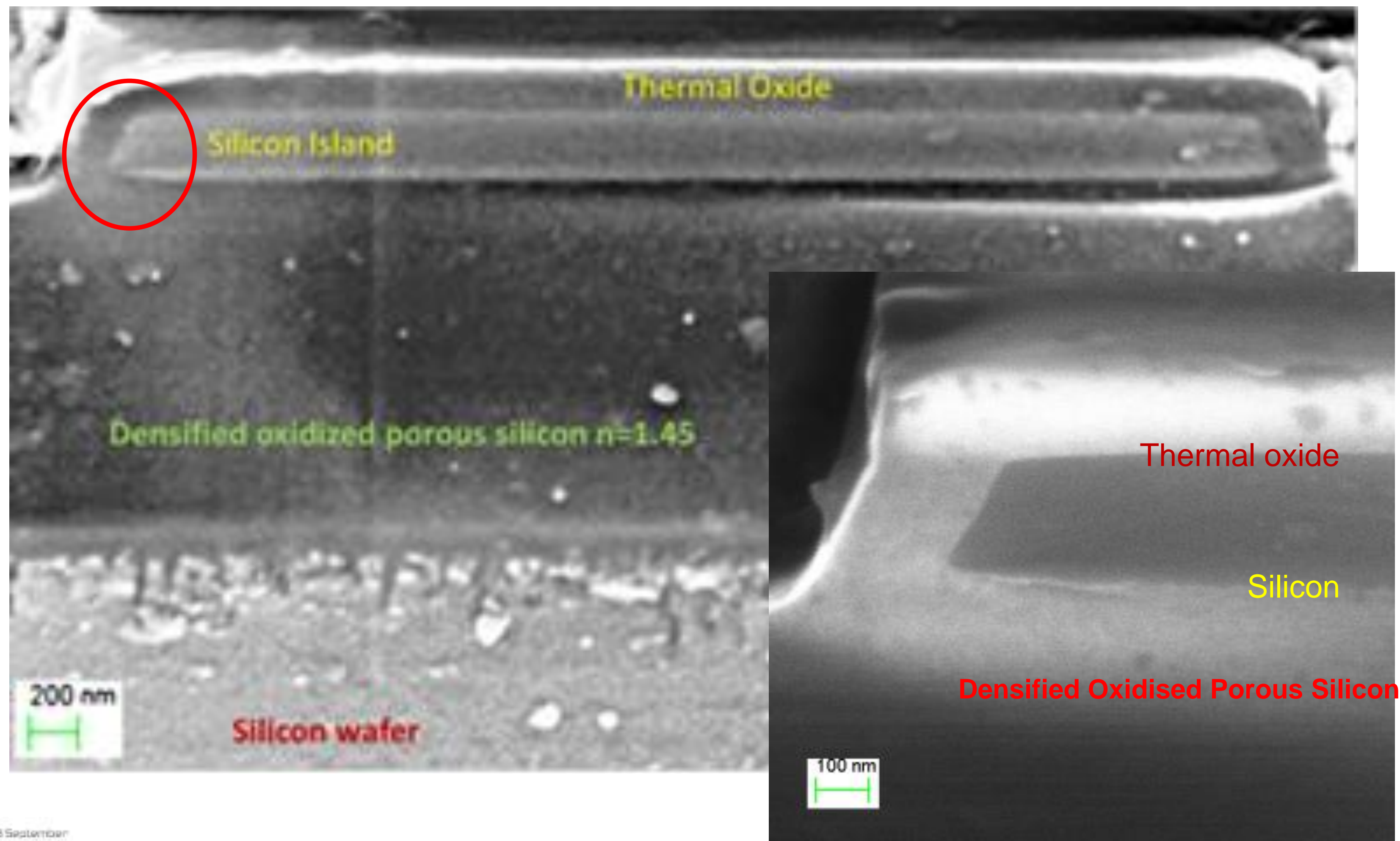
RIE – 10 nm, oxidation – 1 nm





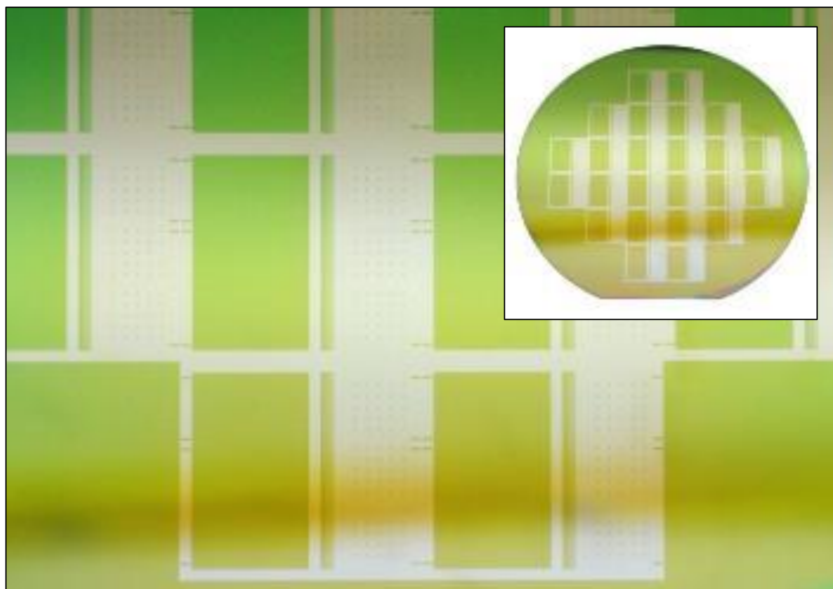
Results and ongoing work

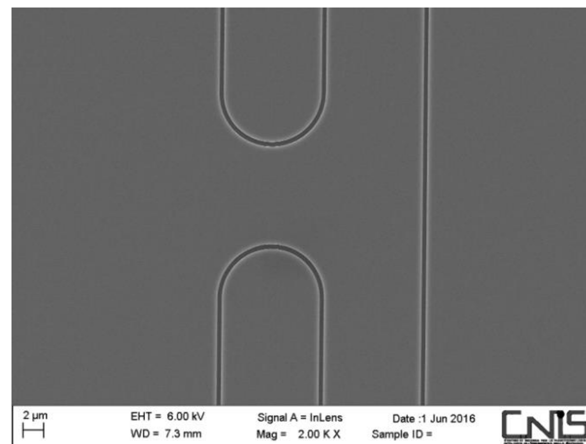
- If everything is done well

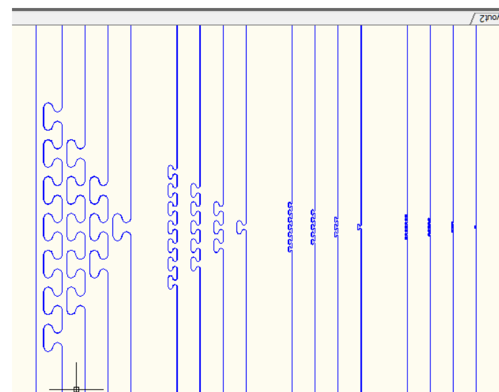


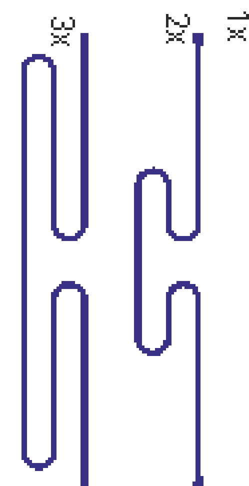
Results and ongoing work: SPWG testing

Test wafer with LSOI-SPWGs arrays for optical characterization









Expected losses of SPWG made on LOPS lower than 0.5 $dBcm^{-1}$ @ 1550nm with 1.5µm OPS

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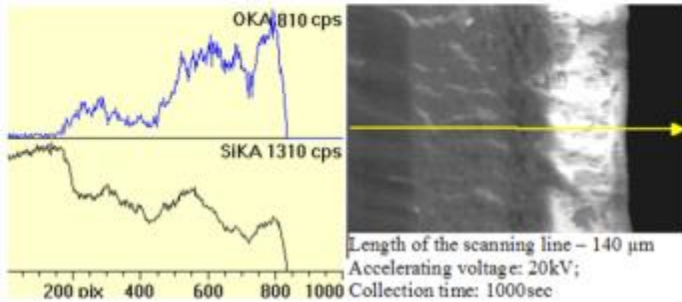
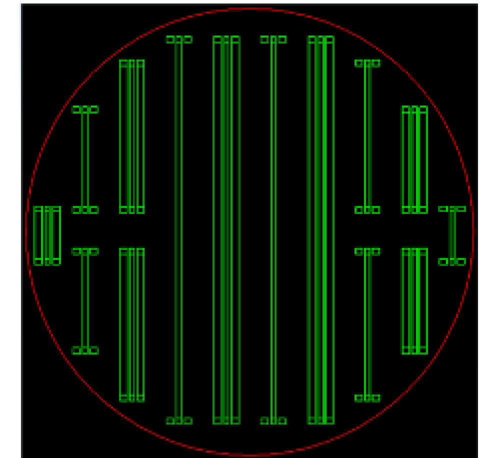
Results and ongoing work: RF decoupling

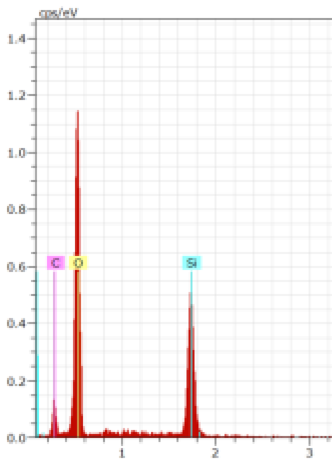
Thick OPS for RF substrate decouplig

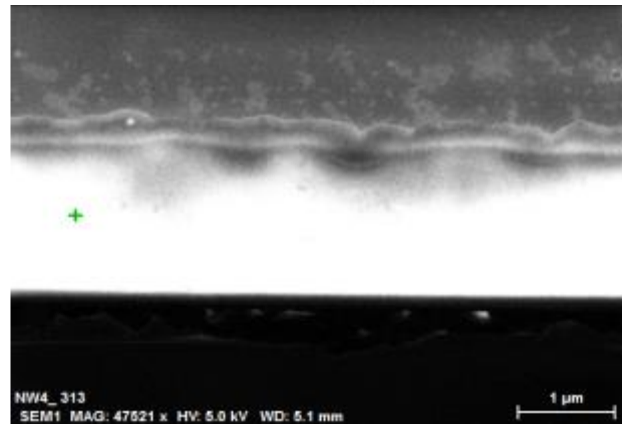


Target reduce losses
on standard CMOS wafer
from
20dB/mm to < 2dB/mm

Designed coplanar RF test WG







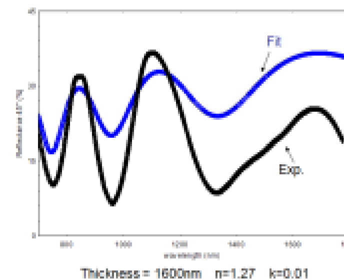
Realised different samples with:

Oxide reference	60 nm
OPS	1 600 nm
OPS	5 000 nm
OPS	10 000 nm
OPS	20 000 nm

Spectrum: Jan 2013_ 107

El	AN	Series	unn. C [wt.%]	norm. C [wt.%]	Atom. C [at.%]	Error (1 Sigma) [wt.%]
O	8	K-series	75.03	51.82	61.65	13.12
Si	14	K-series	60.66	41.90	28.40	3.48
C	6	K-series	9.10	6.28	9.96	3.24
		Total:	144.78	100.00	100.00	

2:1



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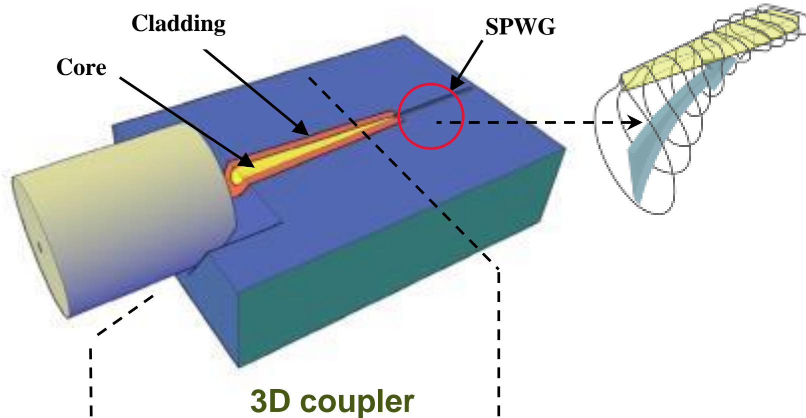
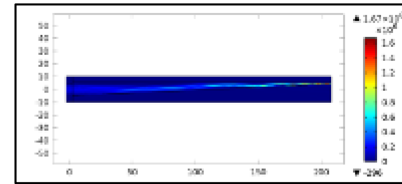
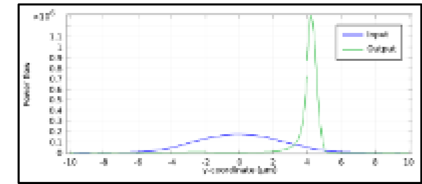
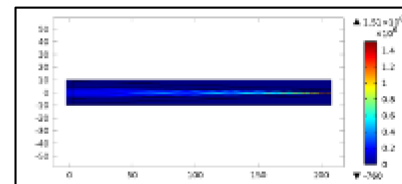
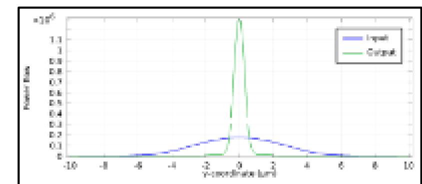
Conference & Exhibition

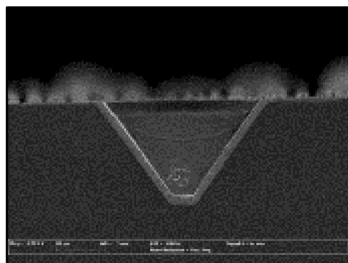
Results and ongoing work: SP and SMF coupling



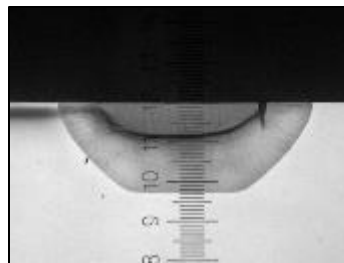
3D coupler

Cross-section and top views of the Gaussian beam propagation



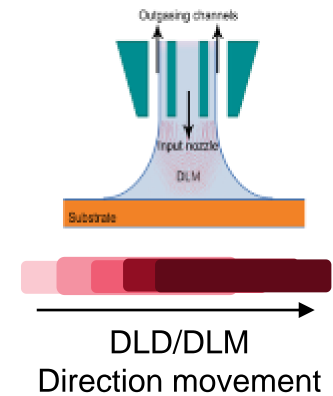
V groove



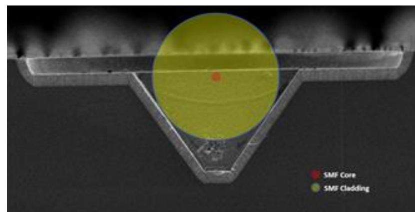
Taper cross-section

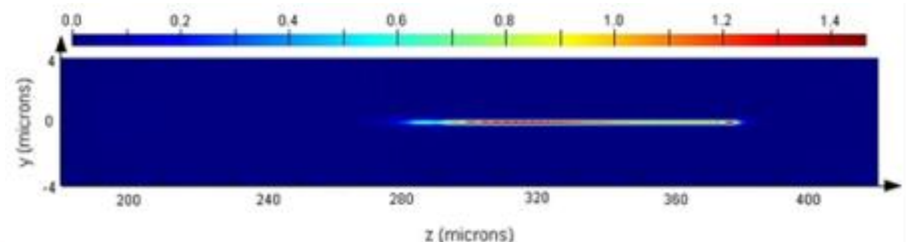
V groove provides rigid alignment

3D refractive index modulation only possible by DLD/DLM



DLD/DLM Direction movement





Summary & Conclusions

- PS or better OPS offers:
  - Buried LOPS modulating TopSi and BOX by ion implantation
  - Thick OPS for RF decoupling
  - OPSWG V-groove coupling
    - PS local formed by DLD/DLM
  - Vertical coupling for VCSEL
  - OPS used as sacrificial layer for MEMS
  - PS used for making Photonic Crystall structures (better OPS)

POROUS SILICON TECHNOLOGY

BY ITS OXIDATION

REPRESENTS A BREACKTROUGH

FOR A REAL SP MONOLITHIC INTEGRATION WITH IC AND MEMS INDEPENDENTLY OF IC TECHNOLOGY NODE

THANKS FOR ATTENTION

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Q&A